Re-host Factors and a Method to Maintain the Integrity of a Test

Larry Kirkland
WesTest Engineering
810 Shepard Lane
Farmington, Utah 84025
801-451-9191 ext 124

Abstract: Re-hosting Test Program Sets (TPS) is a diverse science. Methods of re-host are determined by many multifaceted factors. Some of these factors are: circuit complexity, customer requirements, documentation, optimal circuit coverage, schematics and data availability, existence of and obtainable test specs, legacy TPS History (no-fault-found and could-not duplicate problems or a high quality reliable TPS), quality of unit under test (UUT) data, technology of the TPS (digital, analog, hybrid, etc.), legacy ATEs, Software (SW) development environment, SW tools and translators, interface test adapters (ITA), contractual requirements; mating connectors, test connectors and fixtures and usability and accessibility of existing legacy TPS code. This paper will cover various TPS re-hosting philosophies (see table 1). Also, the paper will discuss the details of using the soft front panel method to duplicate a non-simulated digital legacy TPS.

Re-Host: A TPS Re-host design, development, manufacture, integration and debug for a Line Replaceable Unit (LRU) and Shop Replaceable Unit (SRU) includes the analysis, assessment and improvement of the legacy test program, component fault coverage and diagnostic isolation capabilities. Also, a TPS re-host includes an analysis of Cannot Duplicate (CND) and Re-test OK (RTOK) occurrences.

Terminology such as Cannot Duplicate (CND), Re-test OK (RTOK), No Fault Indicated (NFI), No Fault Found (NFF), and No Trouble Found (NTF), are used to describe the inability to replicate field failures during repair shop test/diagnosis. This paper uses CND to refer to all such failures. On specific Units Under Test (UUTs), CND failures can make up more than 85% of all observed field failures in avionics and account for more than 90% of all maintenance costs. These statistics can be attributed to a limited understanding of root cause failure characteristics of complex systems, inappropriate means of diagnosing the condition of the system, and the inability to duplicate the field conditions in the laboratory.

When a unit is tested outside its' operating system, it has normally been removed due to a fault. The external test may not discover any fault and a CND event may occur. The CND occurrence is a major problem when dealing with complex technical systems, and its consequences may be manifested in system down-time and increased life cycle costs. There are multiple interacting causes of CND, demanding tough requirements for successful solutions. There are ways and technologies that provide possible improvements for the prevention of causes of CND and the reduction of its consequences. The identified causes and solutions are related to life cycle stages, availability performance factors, test technologies, and system stakeholders.

The depot shop or the actual users of legacy TPSs have hands-on knowledge of the quality of the former TPS to be re-hosted. The actual test program expert is the actual user. The user becomes familiar with the program weaknesses and strengths. Often, they can perceive actual component failures based on test program failures without using the diagnostic routine. The user performs actual TPS validation. Validation refers to evaluating system performance to establish compliance with functional requirements and assess system accuracy and correctness by addressing questions such as have we built the right system?; is the system knowledge adequate? Actual using

Table 1
Re-host factors

FACTOR	IMPORTANCE	OBSERVATIONS
Circuit complexity	Critical	ATE resources, >cost, tools
Customer requirements	Critical	Cost, quality, duplicate
Documentation	Deterministic	Depends on contractual requirements, quality of legacy TPS
Optimal circuit coverage	Critical	Quality of legacy TPS, schematics and data availability
Schematics and data availability	Deterministic	Existing TPS code reuse, improving TPS
Existence of and obtainable test specs	Deterministic	Existing TPS code reuse, in-complete
Legacy TPS History	Deterministic	CNDs, RTOKs, type of code, reusable?
Quality of unit under test (UUT) data	Deterministic	Cost, ATE resources, back-trace, manually develop, reverse engineering
Technology of the TPS (digital, analog, hybrid)	Dependent	Simulator, high current, ATE resources
Legacy ATEs, Software (SW) development environment	Deterministic	Reusable, availability, state-of-the-art
Legacy ATE resources	Deterministic	High current, speed, I/O, timing, unique instruments
SW tools and translators	Deterministic	Reusable, availability, state-of-the-art
Interface Test Adapters (ITA)	Deterministic	# of components, type of wiring, can it be duplicated?
Contractual requirements	Critical	Reuse, improve
Mating connectors	Deterministic	Can it be duplicated?
Test connectors and fixtures	Deterministic	Replace, improve, complexity
Usability and accessibility of existing legacy TPS code	Deterministic	Obtainable, digitized, language

domain validation ensures accuracy and completeness of the knowledge base while reliability of system output [1]. Verification, on the other hand, establishes structural correctness and process effectiveness by evaluating the test program for logic; while testing executes a piece of software with the goal of finding errors; actual testing needs to exercise a set of test cases on many paths, although it does not guarantee that each path is tested, functional testing validates problem specifications by comparing system output with known results. Both functional and actual testing are necessary to build reliable test programs[2].

Often customers require the use of existing digital stimulus patterns when re-hosting a non-simulated TPS. These patterns were not simulated but rather applied to the circuit under test and the response monitored. Pattern sets of legacy TPSs have often gone through cycles of adjustments to solve problems.

Quality: The principle rules for determining the quality of a legacy TPS are:

- Are RTOKs or CNDs or NFF or NTF a problem?
- Are the Diagnostics correct?
- Have the big bugs been eliminated?
- Are there glitches in the program?
- When you have a failing test is the information presented correct?
- When you find a bug, is it easy to identify?
- Are there obscure bugs in the code?
- Does the program track consistently?
- Is it straightforward to chase down obscure bugs in the code?
- Is the program cumbersome and unintuitive?
- Can you break the code?
- How you experienced a hiccup in the program?
- Have you experienced random anomalies?

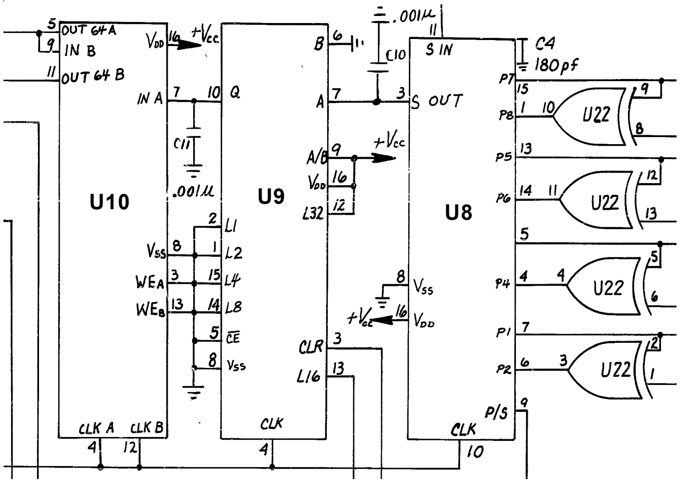
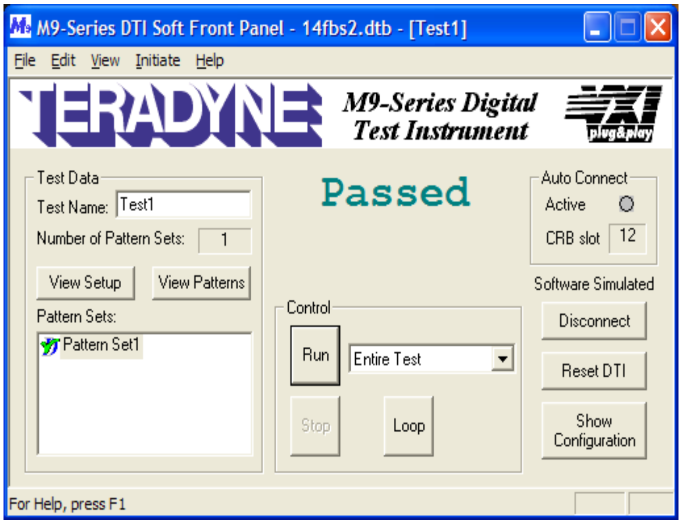


Figure 1. Sample Circuit

Tried and Tested: Duplicating a tried and tested set of patterns can guarantee a quality test and ensure the circuit under test is properly tested. If the integrity of a non-simulated digital test needs to be maintained, a soft front panel test can be developed. The patterns can then be applied to the circuit under test and the results verified. Figure 1 is an example of a part of a semi-complex non-simulated circuit with a quality set of digital patterns. Should a failure be encountered, then a probing routine is generally activated to fault isolate to a specific part.

Figure 2 is the soft front panel display for the UUT test. Figures 3 and 4 show how parameters are adjusted in the soft front panel to stabilize the primary output pins. Prior to testing, the output pins are set to a logic zero. When the test is performed, the soft front panel has the option to find the failing pins. Once the failing pins are located, they are changed to a logic high state. Then the test is repeated to verify stability. If the test is stable, it is best to perform a loop of approximately 1000 times on two or three known good UUTs. The soft front panel will indicate any failures in the looping routine. If a failure should occur, the parameters like the level and timing will need to be adjusted and the looping test repeated. Once the looping test is absolutely stable, then the go-path test is complete. The go-path pattern set is shown in Figure 5.


M9-Series DTI Soft Front Panel - 14fbs2.dtb - [Test1]

Test Data

Test Name: Test1

Number of Pattern Sets: 1

Pattern Sets: Pattern Set1

Passed

Auto Connect

Active ○

CRB slot 12

Software Simulated

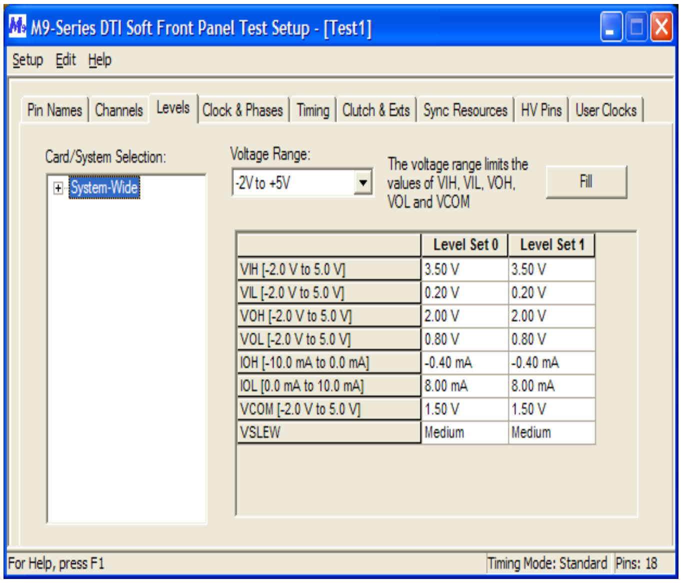
Control

Entire Test

For Help, press F1

Figure 2. Soft Front Panel

The soft front panel test can be precisely developed by adjusting parameters like: levels (VIH, VIL, VOH,VOL), clocks and phases, timing, etc. Initially adjusting these parameters is advisable to setup a theoretical stabilize circuit response. This method is very reliable for testing circuits that were never simulated. If a failure should occur in go-path integration, then these parameters should be adjusted. Care must be taken when adjusting parameters, it is advisable to adjust one or two parameters then rerun the test to determine the effect. It might take several tries to optimize the parameter set, be careful not to over-adjust the parameter set. Use your skill and circuit knowledge to set the parameters, skewed parameters can cause problems with the quality of the test.


M9-Series DTI Soft Front Panel Test Setup - [Test1]
Setup Edit Help
Pin Names | Channels | Levels | Clock & Phases | Timing | Clutch & Exts | Sync Resources | HV Pins | User Clocks
Fill

Card/System Selection: System-Wide

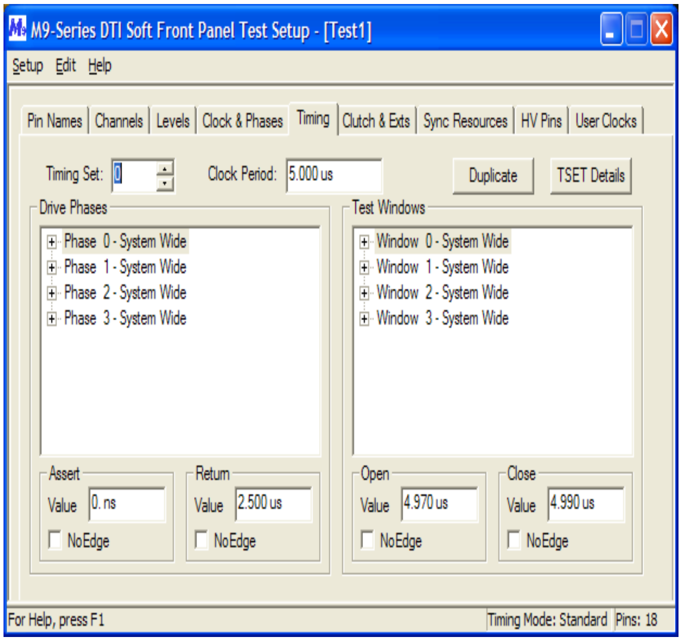
Voltage Range: -2V to +5V

The voltage range limits the values of VIH, VIL, VOH, VOL and VCOM

	Level Set 0	Level Set 1
VIH [-2.0 V to 5.0 V]	3.50 V	3.50 V
VIL [-2.0 V to 5.0 V]	0.20 V	0.20 V
VOH [-2.0 V to 5.0 V]	2.00 V	2.00 V
VOL [-2.0 V to 5.0 V]	0.80 V	0.80 V
IOH [-10.0 mA to 0.0 mA]	-0.40 mA	-0.40 mA
IOL [0.0 mA to 10.0 mA]	8.00 mA	8.00 mA
VCOM [-2.0 V to 5.0 V]	1.50 V	1.50 V
VSLEW	Medium	Medium

For Help, press F1 | Timing Mode: Standard | Pins: 18

Figure 3. Levels


M9-Series DTI Soft Front Panel Test Setup - [Test1]
Setup Edit Help
Pin Names | Channels | Levels | Clock & Phases | Timing | Clutch & Exts | Sync Resources | HV Pins | User Clocks
Duplicate
TSET Details

Timing Set: 0

Clock Period: 5.000 us

Drive Phases
- Phase 0 - System Wide
- Phase 1 - System Wide
- Phase 2 - System Wide
- Phase 3 - System Wide

Test Windows
- Window 0 - System Wide
- Window 1 - System Wide
- Window 2 - System Wide
- Window 3 - System Wide

Assert: Value 0. ns ☐ NoEdge

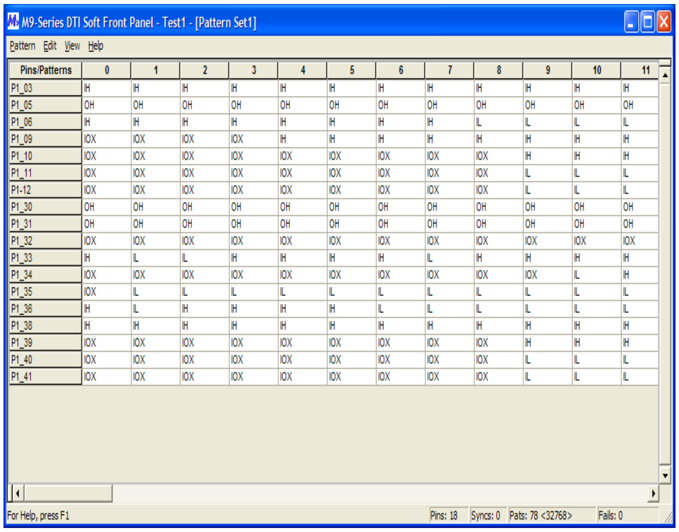
Return: Value 2.500 us ☐ NoEdge

Open: Value 4.970 us ☐ NoEdge

Close: Value 4.990 us ☐ NoEdge

For Help, press F1 | Timing Mode: Standard | Pins: 18

Figure 4. Timing

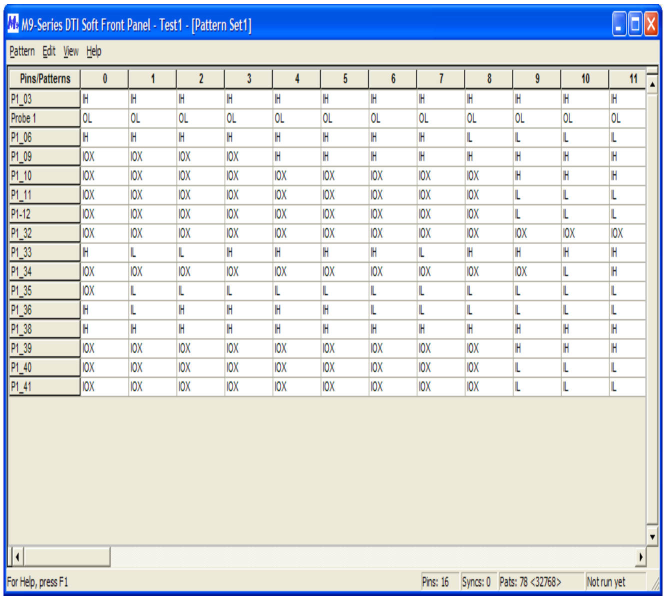


Pins/Patterns	0	1	2	3	4	5	6	7	8	9	10	11
P1_03	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH
P1_05	OH	OH	OH	OH	OH	OH	OH	OH	OH	OH	OH	OH
P1_06	IH	IH	IH	IH	IH	IH	IH	IH	IL	IL	IL	IL
P1_09	IOX	IOX	IOX	IOX	IH	IH	IH	IH	IH	IH	IH	IH
P1_10	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IH	IH	IH
P1_11	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IL	IL
P1-12	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IL	IL
P1_30	OH	OH	OH	OH	OH	OH	OH	OH	OH	OH	OH	OH
P1_31	OH	OH	OH	OH	OH	OH	OH	OH	OH	OH	OH	OH
P1_32	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX
P1_33	IH	IL	IL	IH	IH	IH	IH	IL	IH	IH	IH	IH
P1_34	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IH
P1_35	IOX	IL	IL	IL	IL	IL	IL	IL	IL	IL	IL	IL
P1_36	IH	IL	IH	IH	IH	IH	IL	IL	IL	IL	IL	IL
P1_38	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH
P1_39	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IH	IH	IH
P1_40	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IL	IL
P1_41	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IL	IL

For Help, press F1 | Pins: 18 | Syncs: 0 | Pats: 78 <32768> | Fails: 0

Figure 5. Pattern Set with Primary Output Pins

Diagnostics can be performed by using the same go-path stimulus pattern set. However, the primary output pins are replaced with a single selected probe point. It is good to identify the probe pin as a probe point for easy identification as shown in figure 6. The probe pin is labeled as "Probe 1."



Pins/Patterns	0	1	2	3	4	5	6	7	8	9	10	11
P1_03	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH
Probe 1	OL	OL	OL	OL	OL	OL	OL	OL	OL	OL	OL	OL
P1_06	IH	IH	IH	IH	IH	IH	IH	IH	IL	IL	IL	IL
P1_09	IOX	IOX	IOX	IOX	IH	IH	IH	IH	IH	IH	IH	IH
P1_10	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IH	IH	IH
P1_11	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IL	IL
P1-12	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IL	IL
P1_32	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX
P1_33	IH	IL	IL	IH	IH	IH	IH	IL	IH	IH	IH	IH
P1_34	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IH
P1_35	IOX	IL	IL	IL	IL	IL	IL	IL	IL	IL	IL	IL
P1_36	IH	IL	IH	IH	IH	IH	IL	IL	IL	IL	IL	IL
P1_38	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH	IH
P1_39	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IH	IH	IH
P1_40	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IL	IL
P1_41	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IOX	IL	IL	IL

For Help, press F1 | Pins: 16 | Syncs: 0 | Pats: 78 <32768> | Not run yet

Figure 6. Probe Point 1 DTB file

We could spend several thousands words and 20 to 30 individual papers discussing probe point selection routines. The probe points sequence can be selected using a logical interpretation of circuit flow, nodal pattern data and topological circuit information. However, we want to discuss how to program the selected probe points. The same routine used for the go-path development is used for each probe point. The soft front panel is used to adjust parameters like: levels (VIH, VIL, VOH,VOL), clocks and phases, timing, etc. Initially these parameters are setup the same as the go-path. The go-path parameter setup should work for each probe point. If a problem is encountered it might be wise to re-examine the go-path parameters. Again, care must be taken when adjusting parameters, it is advisable to adjust one or two parameters then rerun the test to determine the effect. It might take several tries to optimize the parameter set, be careful not to over-adjust the parameter set. Use your skill and circuit knowledge to set the parameters, skewed parameters can cause problems with the quality of the probe point test.

The first probe point is shown in Figure 7. The standard back-trace probing test is used once a failure pin is identified. If the probe one test fails, then the TPS can be directed to probe U9 pin 10. Another probe file needs to be created to probe U19 pin 10. If U9 pin 10 passes then U10 is called-out as the probable cause of failure. Since the circuit shown has the WEa and the WEb grounded it is easy to test.

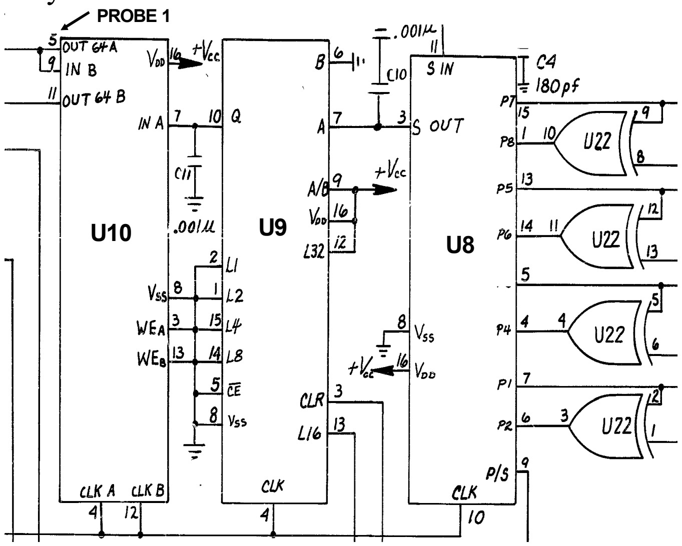


Figure 7. Probe Point 1

Circuit complexity and how it is wired became factors in choosing this method for test. This is just one of many methods that can be used to test a circuit. The selection of a method for test is vital to streamline the TPS re-host and to optimize the quality of a test.

Conclusion: With current generation and next generation test systems focusing on testing efficiency, it is critical to develop test strategies or methods that maximize testing throughput, make better use of the increasingly expensive instruments used in test station and drive down test costs.

Test Strategy analysis should include evaluating existing legacy code, at times it might seem the legacy code does not seem to properly examine Input/Output pin coverage, component failure mode coverage and ambiguity group size assessment. However, legacy TPSs test strategy often is based on factors unbeknownst to the re-host test engineer. It is good to question a test strategy, but if a test sequence is of good quality and does the job, it should be used.

References

1.Benbasat, I., Dhaliwal, J. S. A framework for the validation of knowledge acquisition. Nowledge Acquisition 1*, 1, (1989), 215-233.*

2.Adrion, W. R., Branstad, M. A., Cherniavsky, J. C. Validation, verification, and testing of computer software. *Comput. Surv 14*, 2, (June 1982), 159-192.