When Should Intermittent Failure Detection Routines be part of the Legacy Re-Host TPS?

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ABSTRACT - Intermittent failures are failures that do not manifest themselves all the time. The fact that they are sometimes there and sometimes aren't can make them very difficult to analyze.[1] Some of the most difficult to diagnose faults are intermittent. It is very difficult to isolate intermittent faults which occur with low frequency.[2] Intermittent electrical faults, as a rule, are notoriously difficult to detect. Sometimes an intermittent short or open circuit may leave visible signs of overheating or micro-arcing on a printed circuit board or a connector, but at other times damage may be on such a microscopic scale that it is likely to go undetected.[3] The inability to find anything wrong by trying to reproduce the incident is no guarantee of the detection of an intermittent fault.

This paper will discuss various ways to detect intermittent failures. The paper will discuss the root causes of intermittent failures. Also, a discussion will take place that addresses why we must pursue new techniques, methods and technologies to detect elusive failures.

I. INTRODUCTION

We need to focus on the exact cause of a failure and perform prognostics during the test and repair cycle. An intermittent failure, in reality, is a failure that occurs periodically and is dependent on a specific set of circumstances. The occurrence of these circumstances might be from a single condition or from multiple conditions. Again, it is necessary to know the minimum set of conditions needed to make the intermittent failure mode observable during test and diagnosis.

Detecting intermittent faults is an elusive science, since there are so many variations and causes. It might be virtually impossible to say one intermittent detect routine will detect all intermittent failures. This paper will contain several suggestions as to how to detect an intermittent failure during Automatic Test equipment (ATE) testing. Certain author defined terms or procedures for intermittent failure detection are:

- Signal Looping
- Pattern Looping
- Signal Stepping
- Frequency Deviation
- Pattern Adjustment in critical areas
- Signal Strength Variation
- Current Path Duplication
- Measuring Capacitance Variations
- Vcc Adjustments
- Resistive/Impedance Rebounce
- Temperature Change Application
- Noise Dissimilarity Testing
- Etc.

The meaning of these terms and the "how to" perform these procedures will be discussed. Also, other ideas about detecting intermittent faults will be discussed and referenced.

The exact cause of an intermittent failure may never be found or figured out. Some of the causes of an intermittent failure could include one or more of the following:

- Substrate Crack
- Structural Integrity Weakness
- Floating Lead
- Molecular Breakdown
- Temperature Sensitive Defect
- Material Degradation
- Loose or Partial Connections
- Poor Solder Joint
- Circuit Damage
- Corrosion
- Irregular or Altered Current Path
- Material Transformation due to Environment
- Others

The circumstances manifested by an intermittent failure may never be isolated but certainly we can speculate and attempt to resolve the root cause.

It is necessary to know the minimum set of conditions needed to make the failure mode observable in a reasonable amount of time. Some intermittent failures are manifested with the application of extreme temperature (usually elevated) to the device. Other failures may become visible with the application of bias conditions bordering on datasheet spec-limits; however an application of bias in the presence of a high temperature can prove disastrous. Hopefully, once the analyst has determined these conditions and has set them up, the device should exhibit its failure. Failure analysis from thereon will simply be the same as conventional failure analysis for a hard failure.

A patent by Kimseng[4] presents a picture of a harsh environment as described below:
"The combination of moisture with corrosive fumes constitutes a particularly severe problem because it can create conductive paths on insulating surfaces. This means that conductive paths exist where none are desired. This is most troublesome in high impedance circuits. Ordinarily solid state circuits operate at low impedance levels and are relatively tolerant of moderate leakage. However in some applications high impedance circuits are called for and these constitute a particular problem."

II. Detecting Intermittents

As shown in figure 1, signal looping and pattern looping are similar.

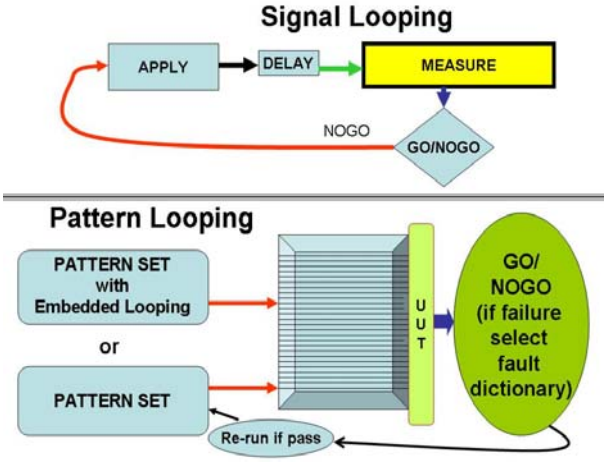

Figure 1. Signal and Pattern Looping

Signal looping can be programmed in with a specific number of loops or it can be programmed using a while statement. The While statement can be setup to monitor a user changeable variable; this is dependent on the test executive's ability to control testing.

Signal stepping can be characterized as a signal tested during ramp up stimulus. Ramp up stimulus is shown in Figure 2. The main characteristic of this technique is the application of a signal until the measurement falls within a certain range. This could be adjusted such that the range could be set on the limits of chip specifications so as to exercise the chips at the peak of their performance. This type of testing does not weaken the component as long as specifications are not exceeded. It must be noted that the test is aborted or fails if the output measure exceeds a specified threshold. You need to keep a tight measurement monitoring test when doing this type of testing so that circuit damage does not occur. It is advisable not to ever exceed maximum specs but rather only approach the specs. Signal stepping can show weaknesses at certain levels. An intermittent can be linked to specific signal levels.

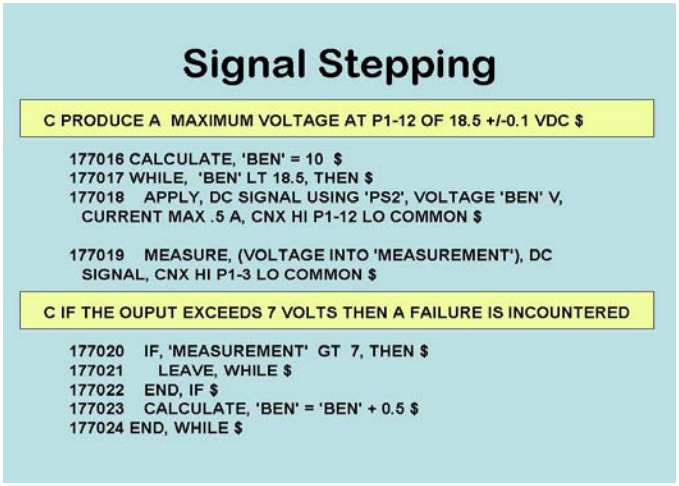

Figure 2. Signal stepping

Frequency Deviation is similar to signal stepping. Frequency deviation is the application of frequency in a semi-random sequence. The idea here is to monitor circuit changes due to a capacitance effect which might be caused by shorts or opens. The deviation can be programmed to what the Test Program Set(TPS) developer feels exercises the circuits properly for failure detection. Figure 3 is merely an example of code that might be used. Frequency deviation is somewhat unique but it must be setup to achieve optimal results. Variations to this type of testing are subject to the developer's findings during integration testing.

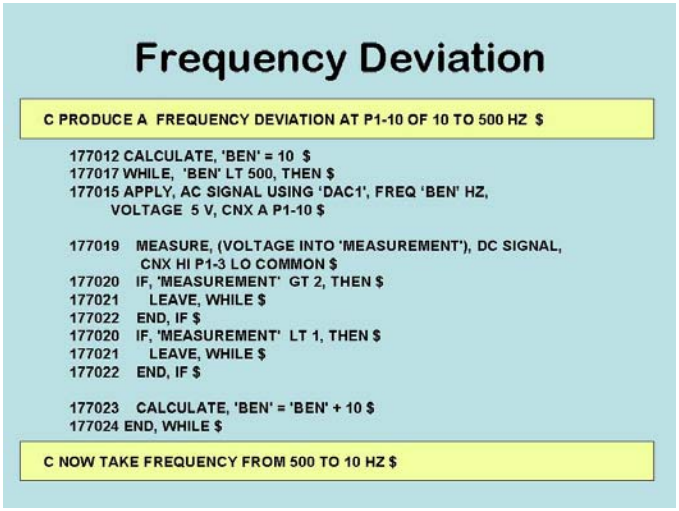

Figure 3. Frequency Deviation

Pattern Adjustment in critical areas involves honing in on the pattern sequence that exercises the specific components in a circuit that experience intermittent failures. This involves a prior determination of an intermittent failure and the component(s) that seem to be prone to this type of failure. If you are using LASAR, you can check the stimulus and response pins during the pattern sequence to verify logic paths and components being tested. Once you have determined the pattern numbers or sequence that exercise the component(s) prone to intermittent failures then add duplicate patterns.

Change the duplicate patterns so that a more robust on/off stimulus is applied. This can cause the output to periodically fail if an intermittent fault is present. Remember, the actual adjustment of these duplicate patterns should be determined during integration testing by the TPS developer. When performing this type of testing for intermittent failures you will need to use the fault dictionary approach to diagnostics.

Signal Strength Variation is similar to signal stepping. However, signal strength variation is not isolated to changing the input voltage but also includes changing the current. You will be adjusting two parameters (voltage and current) to test for intermittent failures. A higher or lower voltage coupled with a higher or lower current has the potential of showing weak circuits. You can raise the voltage and lower the current or vise versa. As with the other techniques, you will need to devise the best method of voltage and current adjustment during integration.

Current Path Duplication is a technique to track the current through a circuit. This technique involves testing for an abnormal current path using a resistive and/or voltage technique. This technique is employed when testing the output of a circuit path by also testing the output of a path by which current might flow during the same test. If an unusual measurement should occur at the duplicate pin this can be an indication of an intermittent failure. This type of testing is very unusual and can produce unstable results. If during integration testing, outputs are not repeatable on known good circuits in the duplicated path then it is not recommended you use this technique. Current flow has always been a source of discussion and interpretation. Current has a tendency to vary for many reasons, so this type of testing must be thoroughly evaluated prior to usage.

Measuring Capacitance Variations consists of many different methods. There are patents and papers that provide techniques for this type of testing.

If the stray capacitance is large enough to worry about in normal operation a typical LCR meter will measure it. An AC excitation is necessary for sensing capacitance variations in stray capacitance. If your stray capacitance is minor you may need a more sophisticated piece of lab equipment. A LCR meter (Inductance (L), Capacitance (C), and Resistance (R)) is a piece of test equipment used to measure the inductance, capacitance, and resistance) of a component. In the usual versions of this instrument these quantities are not measured directly, but determined from a measurement of impedance. The necessary calculations are, however, incorporated in the instrument's circuitry; the meter reads L, C and R directly with no human calculations required.

As an example, LCR meters, capacitance meters, resistance meters, and impedance analyzers are useful in testing components and materials in a variety of research and design applications and in component manufacturing. LCR meters measure impedance (inductance, capacitance, and resistance) at spot frequencies. Capacitance meters measure capacitance at spot frequencies. Resistance meters are optimized for high-resistance or low-resistance measurements. Impedance analyzer is the most powerful tool to measure impedance (inductance, capacitance, and resistance) across a range of frequencies[5].

The Vcc Adjustments technique is employed by adjusting the component(s) normal bias voltage. You must not exceed the chip manufacturer's specifications (example is shown in Table 1). The Vcc adjustment technique might show output variations from intermittent components as compared to stable components. By adjusting Vcc you can monitor the output signal pins/paths of intermittent failure circuits and determine if this can be used to identify defective components. This method requires thorough integration testing and verification.

Operating conditions SN5404 VCC SUPPLY VOLTAGE		
MIN	NOM	MAX
4.5	5	5.5

Table 1. VCC Specs

Resistive/Impedance Rebounce is a technique very similar to Measuring Capacitance Variations. Resistance meters can be optimized for high-resistance or low-resistance measurements. An impedance analyzer is the most powerful tool to measure impedance (inductance, capacitance, and resistance) across a range of frequencies. It is important to note the adjustment of frequency. The actual frequency range needs to be determined during integration testing.

Temperature Change Application is exactly as the name suggests. It is the technique of exposing the Unit Under Test(UUT) to various temperatures during testing. Remember, cold temperatures possibly show intermittent failures more than higher than normal temperatures. You can combine intermittent techniques with this technique to achieve optimal results. Remember, to always stay within the specifications for the components on the UUT.

There is a Linear IC Tester with a built-in test library which includes all common Analog ICs including op-amps, comparators, voltage regulators, voltage references, analog switches & multiplexes, opto-isolators & couplers, and audio ICs. A Digital IC Tester has a comprehensive device library covers most TTL, CMOS, memory and interface devices with a 40 pin capability (NAND gates or CPUs) and detects intermittent and temperature related faults and displays diagnostic information for individual pins. Testers are able to locate intermittent and temperature related faults by using its unconditional or conditional loop testing modes[6].

Noise Dissimilarity Testing is testing for noise variations on the UUT. Monitoring the noise on the Vcc line is always a good idea. However, monitoring the noise of an output signal

on a pin and comparing that noise measurement to the output signal of another pin might show component weaknesses. It is a wise choice to look at noise on UUTs that have intermittent failures. Noise can be a decisive factor and tends to get amplified on weak circuits. Noise can be measured by any quality instrument capable of measuring an AC frequency.

III. Circumstances manifested

Intermittent circumstances for IC components could include the faults shown in Table 2. This table is not fully comprehensive but it is used to illustrate problems that might occur and require critical test techniques and test parameter settings. It most be noted that the quality of the test equipment is always a factor when testing for intermittent failures. Weak test equipment with low parameter adjustments hinders testing for intermittent faults. Circumstances are vast and can vary significantly. The important fact relating to testing is to use tight parameters and use high quality test equipment.

Causes	Failure Modes	Interpretation
Threshold voltage shifts	Increased gate delays Slow-to-fall signals	Intermittent or random on ATE, test setup is critical
Weakened drive gates	Increased gate delays Slow-to-rise/fall signals	ATE test parameters critical, requires high quality ATE
Shorts - Defective interconnects	Degraded signals Increased gate delays Increased RC delays Increased leakage Opens	ATE test setup is critical, must have tight settings
High/low resistance interconnects	Increased RC delays Slow-to-rise signals Slow-to-fall signals	Tight rise and fall measurements required
Passageway opens	Fails at high frequencies	Frequency span testing is critical

Table 2. Intermittent Circumstances

IV. Conditions and observation

Intermittent failures are manifested in various ways or set of conditions. We need to setup the minimum set of conditions needed to make the failure mode observable in a reasonable amount of time. After the determination of these ways or these conditions has been setup, the intermittent device could exhibit its failure. Failure analysis from thereon will simply be the same as conventional failure analysis for a hard failure. Setting up these ways and conditions can be very difficult.

I'm not a fan of people that excuse their responsibility to fix a No-Fault-Found (NFF) problem by saying the failure is intermittent and can not be tested by ATE. When determining what TPS changes are required to fix an NFF problem the engineer should have a wide variance of testing options to resolve the problem. If we don't advance our testing options as technology advances then we are not staying up to date with technology. Also, the engineer should always employ their inventiveness when determining a method for intermittent fault detection. I know from experience that engineers are highly inventive, as a matter of fact; an engineer is actually paid to use their inventiveness (that is what an engineer does).

Of course, aging occurs over time. Aging is caused by repeated exposure to the environment. It could be perceived that it is rare for aircraft components to be fully functional one moment then completely faulty (hard failure) the next moment. A phase of intermittency can occur, but this is UUT dependent. Intermittent failures are not easily detected with traditional test equipment because of their random and often infrequent in nature.

Intermittent failures classifications are:

- Randomly fails
- Can be perceived as SYSTEM failures that ATE does not normally detect
- If mainline can't detect the problem then, diagnostics can not work.
- The inability to reproduce the symptom during maintenance/diagnostic activity.
- The inability of test equipment to detect the root causes of intermittent, randomly-occurring faults.
- The lack of availability or lack of access to, relevant corporate technical knowledge.

V. Root causes

Intermittent failures are not easily detected with traditional test equipment because of their random and often infrequent nature. A No Fault Found (NFF) is a reported fault for which the root cause cannot be found, see figure 4. The No Fault Found, Can Not Duplicate, No Evidence of Failure and No Problem Found can be caused by either an intermittent failure or a hard failure.

Hard failures can manifest themselves as intermittents in the next higher assembly. This is due to function or circuits being accessed at any given time. Some of the monitoring can be isolated to an output of a certain range and this range can be in spec until another function is selected. There are many variations associated with the BIT test. Noise and VCC variations can produce BIT failures. Potential false alarms do actually occur in built-in-test systems even though it is not generally discussed or realized. Testing accuracy can be deceiving at all levels of test. Random BIT failures are not particularly considered in the overall equation when tracking intermittents.

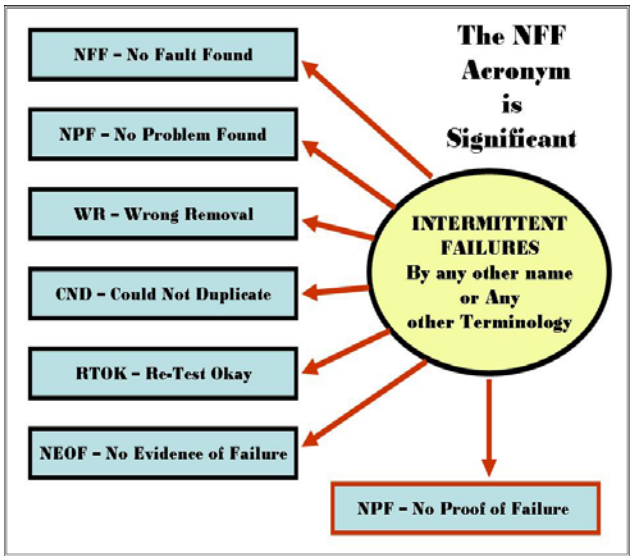

Figure 4. NFF by any other name

No matter what name is used to describe an intermittent failure, the fact is an intermittent failure is a failure that cannot be duplicated during ATE testing using standard test routines. The diagnostic investigation becomes academic if the actual root cause of the fault cannot be isolated. The fault is the inability of the ATE to fulfill its intended function. NFF terminology is a diagnostic failure as shown in figure 5.

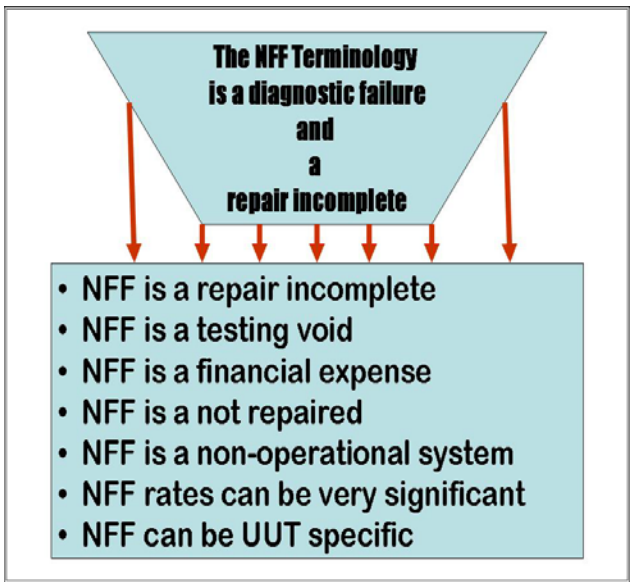

Figure 5. NFF Terminology

Some of the factors associated with failures in fault diagnosis and root cause analysis include: the inability to reproduce the symptom during maintenance/diagnostic activity, the inability of test equipment to detect the root causes of an intermittent, randomly-occurring faults and the lack of availability of, or lack of access to, relevant corporate technical knowledge.

If you manufacture, operate or maintain critical electrical and electronic systems - whether as part of an aircraft, or a satellite ground station - then you need the confidence and assurance that these systems will continue to carry out their intended function correctly and safely throughout the entire duration of their intended usage and life-cycle. This is called "System Integrity". [7]

Problems with System Integrity present themselves in a variety of guises such as:

- Intermittent Faults
- No Fault Found
- Wiring Integrity problems
- Age-related Failures [7]

The NFF chain of events could be as follows:

- It is a chain of events that starts, chronologically, with the end user experiencing a fault symptom.
- The chain of events might progress from a sortie abort to reporting of the fault to the relevant technicians, through to diagnosis and rectification activity.
- If the diagnosis is a success then the genuine root cause of the fault is isolated and rectified and the aircraft is signed off serviceable having been made fit-for-purpose and airworthy once more.
- However, if the root cause cannot be found – in other words, the activity has resulted in *diagnostic failure* – you are dealing with a NFF situation[8].

In test/diagnosis the root cause of an intermittent failure is the actual component or connection that causes the failure. The engineer needs to track down the root cause of a failure prior to changing the TPS. Sometimes a failure simply cannot be detected by testing, so some kind of originality should be employed.

An example of originality is:

- Add a simple question to the TPS and ask what failed on the weapon system,
  - Did the green tag specify "Failed the Oscillator Test"?

True/False - Add an R/R based on the weapon system failure.

You could even inform the user to change a specific component if a NFF is occurring. By experience, it has been shown that NFFs for a specific UUT usually occur on the same component(s) or connection. Also, you should try to eliminate the occurrence of the intermittent failure by determining what actually caused the failure on the weapon system.

The reasons why intermittent failures might occur in a UUT include (but not limited to) the following:

- Proximity to extreme cold or heat

- Poor circuit design
- Specific chip types
- Specific chip manufacturers
- UUT location in the weapon system
- Poor repair
- Poor solder
- Improper handling
- Excessive vibration
- Prolonged use
- Environmental Conditions
- Corrosive Substances
- Corrosive Conditions
- Etc.

Some intermittent failures are manifested with the application of extreme temperature (usually elevated) to the device. Other failures may become visible with the application of bias conditions bordering on datasheet spec-limits; however an application of bias in the presence of a high temperature can prove disastrous. Hopefully, once the analyst has determined these conditions and has set them up, the device should exhibit its failure. Failure analysis from thereon will simply be the same as conventional failure analysis for a hard failure.

Can you turn an intermittent against itself? "I once worked with an electronic tech who, well, let's just say he'll never compete with Einstein. The low frequency model of a transistor was a little more than he could handle. But give this guy an intermittent, and he'd fix it in no time. Simple. He'd wiggle everything, use a heat gun and freon to toggle the temperature, and wait for it to happen. He'd slowly narrow the wiggling and heating until he could toggle the symptom by manipulating a single component, then replace it. He needed absolutely no electronic theory. Like an Aikido master, he turned his opponent's strength against him."[8] Manipulation, coupled with astute observation, is often the quickest way to solve an intermittent.

VI. TPS and INTERMITTENT FAILURES

There are various questions the TPS developer should consider about intermittent failures. Questions about TPSs and intermittent problems:

1 – Should we ever test for an intermittent?
2 – Should there be a standard set of intermittent tests?
3 – What type of tests should be classified as intermittent detection tests?
4 – Can we (technician/engineer) enter intermittent failure data into the TPS?
    a. Should we approve these entries by a Material Improvement Project?
5 – Can we ask the technician to replace a component(s) based on the next higher level test(s)?
6 - What flexibility can the repair technician have to alter the TPS on-the-fly?
    a. Should they be allowed to enter non-intrusive, text data only information?
    b. Should we allow additional R/R callout information to change on-the-fly?

Overall, this information can be used by the TPS engineer (especially in rehosting) to make the TPS better and more robust.

We need to expand our flexibility and take a close look at what can be done during testing to update the TPS on-the-fly. I understand we must tightly control what the TPS does and what information is presented to the technician. However, we make create routines to verify on-the-fly changes and approve them. It is clear there are still many things we can do better and smarter, it is another case of 'Who's to do it."

If you are Rehosting a legacy Test Program Set (TPS) with a high Retest OKAY(RTOK) or No-Fault-Found(NFF) rate chances are the Unit Under Test (UUT) has an intermittent fault(s). It is interesting to note that certain UUTs are prone to intermittent faults. The fact that certain UUTs are prone to intermittent faults gives rise to the questions:

- What causes the intermittent failures?
- What can I do to the rehost TPS to test for intermittent failures?
- Where are the intermittent failures (component(s))?
- What TPS changes have been performed to detect intermittent failures?

If your TPS looks and feels great but when fielded exhibits:

- High RTOK rates
- High Could-Not-Duplicate(CND) rates
- High NFF rates, then
- In REALITY, you've got problems

These problems should be mitigated at sometime during the life-cycle of the TPS or they should be addressed during the rehost phase. Also, if your TPS shows a 95% detect rate and seems to work as advertised and if your TPS accurately detects a vast array of inserted faults, but when fielded, will not detect actual UUT failures: WHAT CAN YOU DO?

- Look at other techniques or technologies.
- Look at what fails at the next higher level.
  - Correlate high level failures to UUT faults
  - Determine actual fault
  - Take another look at the TPS, if there is an obvious weakness, then fix it, BUT

ALL TOO OFTEN OBVIOUS WEAKNESSES ARE NOT FOUND due to intermittent failures, and, TPS FIXES ARE JUST NOT MADE.

Intermittent fault detection techniques could include but not limited to:

One technique:

- Add a manual question to the TPS and ask what failed at the next higher level,
  - This should be in a specific pointed format:
    - Did the green tag specify "Failed the oscillator Test"? Yes/No
- Add an R/R based on a specific next higher level failure.

Second technique:

- Consider adding a new type of test for the problem, this could require quite a lot of effort.
- Ask the program manager for funding to pursue techniques that might detect the failure
- Explain the testing problem in detail, make a good case and remember to adequately justify.

Remember, problems are not fixed by saying it can't be tested.

VII. PHYSICS

Test technology physics is a science often overlooked. Over time we have come to believe that the standard stimulus and response criterion is a must for circuit diagnosis and for determination of ready to use. Although the standard stimulus and response is part of the equation, it may not be the total solution. Our mandate is to discover and pursue technologies or test techniques to improve the quality of a test and reduce test development cost and time and reduce life cycle costs. We need to do things better, more cost efficiently and improve the quality of a test.

Over-testing, miss-testing, or under-testing can be a result of standard stimulus and response. Things like timing, signal strength, duplicating the operating environment, loading, fan-out, and properly interconnecting the UUT are some factors associated with standard testing.

A defective circuit is like a sickness that needs to be treated. It is one type of analysis that is required to determine that we feel weak and achy, and a completely different type of analysis using intelligence and insight is needed to find the root cause of our ailment. While the former can be achieved simply (anyone can figure out that he/she is ill), the later requires diagnostic insight that doctors train many years to accomplish. In doing so, doctors do not simply rely on the patient's determination, but rather on external diagnostic equipment, such as thermometers, X-rays, Laser Scanners, MRI, robotic nano-technology cameras, etc. We must similarly intertwine our test techniques to fully evaluate the functionality of the Unit Under Test (UUT). At times one cannot simply rely on a single ATE instrument set to find all faults. There are other test techniques that we could turn to such as EME.

Electromagnetic Emission spatial and spectral scans of the UUT are made over various frequency ranges to identify emission sources at the UUT component (electrical, electromechanical and mechanical) and circuit board level. Signatures associated with increased electromagnetic emissions, lack of emissions, and changes in emissions are indicative of potential and actual UUT component failures. This type of testing is non-intrusive, non-hazardous and can offer improved UUT functionality quality and diagnostic capability.

Electromagnetic Emissions Spectral Technology Justification is shown in table 3.

Factor	Justification
TPS Development	Can verify hardware detection, current path and quality of the UUT (re-hosted TPSs are often improved TPSs which detect more UUT component problems).
CNDs	Test and Diagnosis of Bad Actors, No-Fault-Found, Could-Not-Duplicate, Multiple callout diagnostics (determining the actual defective component), focusing on problems with little stimulation or testing, etc.
Fault isolation	Enhancing fault isolation. Conventional test methods can only provide fault isolation to an ambiguity group (driver and sink components). This technology appears to perform fault isolation to the individual component level.
Prognostics	Enhancing UUT prognostics with the detection of marginal components that are operating at the limits of specifications and are likely to fail in the near future.

Table 3. EME justification

Integrating Electromagnetic Emission spatial and spectral scans technology into an actual fielded tester could include at least the actions.

- Develop full-function hardware drivers.
- Develop and code the interface between the EME technology and the ATE computer.
- Add code to the Test Executive option menu to interface with the EME Technology and interpret/display the EME test results on the UUT test display.
- Engineer/develop a sync pulse (extra digital pin) coupled with LASAR pattern segment technology (Judge file relationship) for digital to optimize EME detection.

- Engineer/develop a sync pulse coupled with analog tests to optimize EME detection.
- Engineer/develop a method to pass EME information to and from the Test Executive.
- Develop the test scheme between EME technology and the Test Executive.
- Develop all the critical WesTest Test Executive code to fully control, interface and display EME test results.
- Design a generic EME antenna array for Shop Replaceable Units(SRU) tested on the ATE.
- Develop/Adapt/Design a generic Interface face Adapter (ITA) fixture to hold the generic antenna array in the ITAs.
- Develop and code additional software to account for variations in positioning.
- Develop a generic approach to the SRU UUT component layout display.
- Procure a high resolution camera for UUT picture cross correlation with component EME activity.

The Test Executive menu items are shown in figure 6.

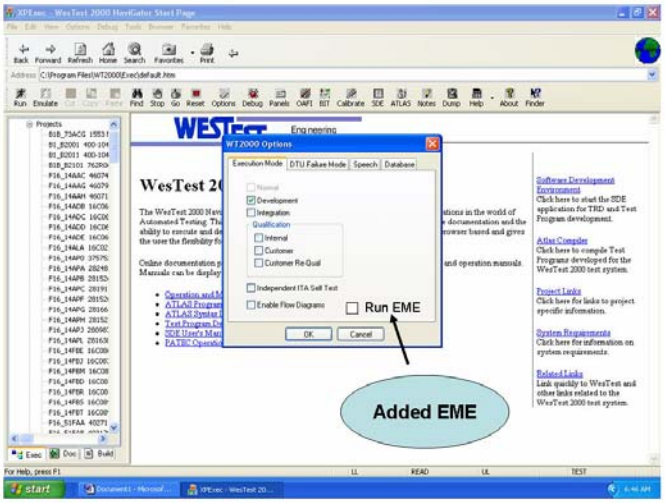

Figure 6. Test Executive EME

Another menu option will then be displayed to select how EME will be performed:

1. Run EME automatically and pass callouts to the TPS
2. Run EME manually using EME menu control

Please enter 1 or 2: _____

You can place a perform statement in the TPS to call the EME application as shown below:

C VOLTAGE SENSOR TESTS IN PROGRESS $
172006 CONNECT, SHORT, CNX HI P1-A4R1-A LO COMMON $
172009 CONNECT, SHORT, CNX HI P1-12-A4R2-A LO COMMON $
172012 CONNECT, SHORT, CNX HI P1-13-A4R3-A LO COMMON $
172015 APPLY, AC SIGNAL USING '3PHASEAC', FREQ 400 HZ,VOLTAGE PHASE-A 115 V, CURRENT PHASE-A MAX .5 A,VOLTAGE PHASE-B 0 V, CURRENT PHASE-B MAX .5 A, PHASE-ANGLE PHASE-B .5 DEG,
VOLTAGE PHASE-C 0 V, CURRENT PHASE-C MAX .5 A, PHASE-ANGLE PHASE-C .5 DEG,
CNX A P1-10 B UNUSEDB C UNUSEDC N COMMON REF PHASE-A $
172018 CONNECT, SHORT, CNX HI P1-6 LO COMMON $
172018 **PERFORM, 'EME' $**
172021 CONNECT, SHORT, CNX HI TP1-5 LO COMMON $
172024 WAIT FOR, 1 SEC $
172027 VERIFY, (VOLTAGE), DC SIGNAL,
UL .4 V LL -.1 V, CNX HI P1-3 LO COMMON $

It is noticed that the EME is performed at a point where the developer feels will give the optimal results. Also, depending on your menu selection you can run the EME during Guided Probe diagnostics.

Also, the Test Executive debug tools can be used to integrate the EME technology in general and in certain places in the TPS. These tools are shown in figure 7.

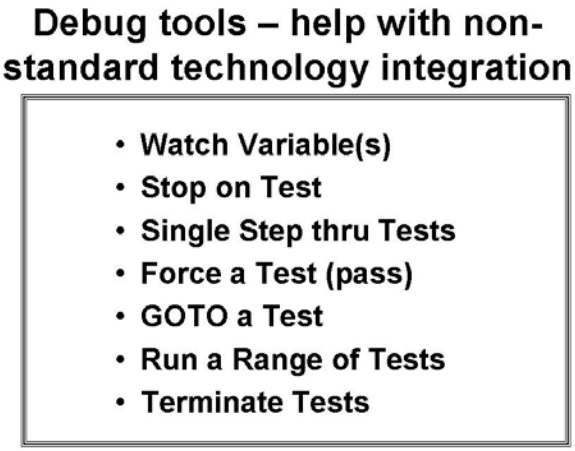

Figure 7. Test Executive Debug tools

You can stop anywhere during testing and run the EME to see the best area for EME testing. Also, the single step, GOTO step, force a test, and run a range of tests is very useful in determining the best placement for EME testing.

Verifying Electromagnetic Emission (EME) spatial and spectral scans technology into an actual fielded tester includes at least the following actions:

- Utilizing the generic EME ITA hardware and EME antenna array on a government furnished ITA.
- Perform actual EME testing using a government furnished ITA(s) and UUT(s).
  - Use an actual UUT test program running on the ATE to verify EME technology.

  - Interact with using personnel for feedback, training, and user requests.
- Develop all the documentation in the WesTest format to use and perform testing with the EME technology on the ATE.
- Design, develop and code any change requests from government personnel.
- To optimize this effort will require testing a digital, analog and hybrid UUT.

EME-based Test Program Development is baselined upon the measurements of a composite of three known good or "golden" UUTs. Post-processing of measured values is performed to identify unique signal signatures of components under known conditions. Diagnostic and prognostic determinations are based upon the presence and/or absence of known signatures, combined with determination of signal flow[9].

The actual potential advantages to adding EME testing is shown in figure 8.

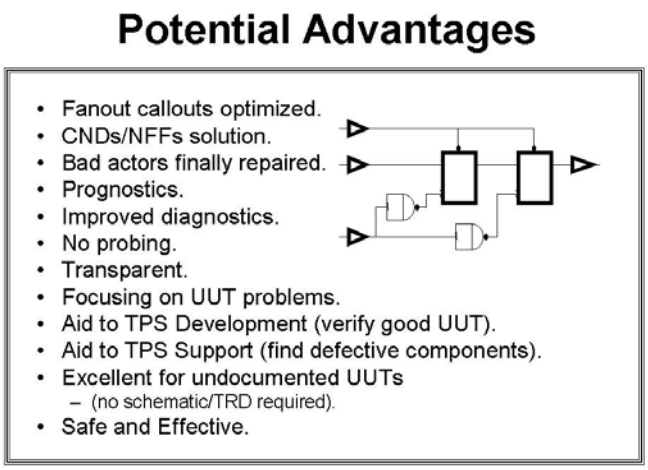

Figure 8. EME Potential Advantages

The bottom line with integrating a new technology is it must meet certain test criteria. Unless this condition is met the new technology quickly becomes useless. We are producing automated technology and we must continue on that path.

There are times when test/diagnosis on certain UUT becomes extremely time consuming and manpower intensive. It is at these times when a new technology can be less automated, however we should never deliver a cumbersome non user-friendly technology. Figure 9 shows the realities that must occur if a technology is to be integrated on an ATE. Essentially the technology should meet the following conditions:

- Technology needed to solve real world problems.
- Technology needed to test some components.
- Technology needed to enhance/add prognostics.
- Technology needed to stay current with new testing techniques.
- Technology needed to fix bad actors and aid in software development and support.
- Bench testing UUTs without ATE (stand alone).
- Technology needed to streamline the repair process.
- Technology needed to determine the actual cause of failure.
- Technology needed to free up ATE usage.
- Technology needed to reduce wear and tear on UUTs.

Figure 9. Integration Realities

The actual physics of circuit functioning should be considered when determining test philosophies. Physics is the most fundamental science. It involves understandings of the basic principles by which all things in the universe exist and operate. It is the natural basis of all the technology disciplines such as electronics, engineering and computer science and, of course, test and diagnosis. While two different boards can both PASS all the ATE tests, their physical characteristics will likely be different. The physics behind those characteristics can help us diagnose the root causes behind the CND and help us repair even those boards that escaped the ATE tests.

VIII. Conclusions

All too often, engineers are faced with testing problems that can not be eliminated due to weak test equipment and/or insufficient information on legacy TPS weaknesses. It is imperative to remember that NFF and RTOK problems are real and do occur on certain UUTs. These problems need to be mitigated by research and at some time eliminated by proper testing, unique information exchanges or adding an instrument and a new test to the ATE and TPS to detect the intermittent failure.

It is well to note that certain intermittent failures at one-level of testing show-up as hard failures. This is due to the fact that the real world operational environment is not exactly duplicated on ATE. There will be differences that can

manifest intermittent failures more rapidly on the actual weapon system.

Not all NFFs are caused by intermittents. There are true test voids that are resolved quite often. Also, there can be a case where an intermittent failure will show a TPS weakness and an additional test will need to be added to resolve the test void.

There is stand alone test equipment to detect intermittent failures. So once you have isolated the intermittent failure including a specific pin on a chip, then possibly you can write a test routine for the ATE to find the intermittent failure. Perhaps you might need to invent a specific routine for the situation. Test engineers are paid to find UUT problems on ATE, so their inventiveness is a job requirement.

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